Development of Analog FE ASIC – HLC1

- R&D of analog FE ASIC in 65nm CMOS technology was started in 2015
  - With final goal of FESOC design including FE+ADC+lpGBT on the same chip
- Two detailed design studies have been presented in LAr Week
  - Dec 2015: https://indico.cern.ch/event/464287/
  - Jun 2016: https://indico.cern.ch/event/537748/
  - Fully differential design with programmable architecture has been simulated extensively and being implemented in the 8-ch HLC1 design
  - Collaborating with Penn on the design of building blocks (pulser, bandgap)
- By mid September
  - The layout design was progressing well, ~85% complete
  - Purchase order of HLC1 submission has been processed

Plan of HLC1 Development

- An arrangement is being worked out with SBU to have Gianluigi continue to work on HLC1 design as an ATLAS collaborator
  - Hopefully the paperwork could be completed within this week
- The goal is to have HLC1 submission in next 3-4 months
  - Integrate the building blocks designed by Penn
  - Continue and finish the layout of 8-ch HLC1
  - Perform post-layout simulation before final submission
  - Projected submission in Jan/Feb 2017
- Design of FETB for digital readout of both HLC1 and LAL/Omega preamp chip has been finalized
  - PCB is being fabricated this week
  - Plan to evaluate both chips in FY17, and provide inputs to LAr TDR draft by the end of 2017
- Next steps
  - Plan to continue the collaboration with Gianluigi while he is planning his career in academia
  - BNL is committed to continue the work of HLC1 in collaboration with Penn